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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
08/765,907	12/17/96	WHITE	L 11-20557

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ART UNIT	PAPER NUMBER
2305	

DATE MAILED: 02/21/97

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No. 08/568,904	Applicant(s) Watts Jr.
	Examiner Rupal Dharia	Group Art Unit 2305

☐ Responsive to communication(s) filed on _____.

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *three* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) *1-31* is/are pending in the application.

Of the above, claim(s) _____ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *1-31* is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☒ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☒ The drawing(s) filed on *Dec 7, 1995* is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Interview Summary, PTO-413

☒ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

Part III DETAILED ACTION

Drawings

1. This application has been filed with informal drawings which are acceptable for examination purposes only. Formal drawings will be required when the application is allowed.

2. The drawings are objected to because Figures 2a, 2b, 2c, 3, 4, and 5 are not designated by a legend such as "Prior Art". The legend is necessary in order to clarify what applicant's invention is. MPEP § 608.02(g). Correction is required.

Claim Rejections - 35 USC § 112

3. Claims 30 and 31 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The term "further **sleeps** a PCI bus" and "further **sleeps** any" is unclear in the context it is used and therefore making the claim vague or indefinite.

Claim Rejections - 35 USC § 101

4. Applicant is advised that claim 12 is a substantial duplicate of claim 13. When two claims in an application are duplicates or else are so close in content that they both cover

the same thing, despite a slight difference in wording, it is proper after allowing one claim to reject the other as being a substantial duplicate of the allowed claim. MPEP § 706.03(k). Therefore, should the indicated claim(s) be found allowable, the duplicate claim(s) will be rejected under 35 USC § 101.

Double Patenting

5. Claim 4 is provisionally rejected under 35 U.S.C. § 101 as claiming the same invention as that of claims 1 and 2, and, 8 and 9 of copending application Serial No. 08/572,202. This is a *provisional* double patenting rejection since the conflicting claims have not in fact been patented.

6. Claim 7 is provisionally rejected under 35 U.S.C. § 101 as claiming the same invention as that of claims 13 and 14 of copending application Serial No. 08/572,202. This is a *provisional* double patenting rejection since the conflicting claims have not in fact been patented.

7. Claim 10 is provisionally rejected under 35 U.S.C. § 101 as claiming the same invention as that of claims 16 and 17 of copending application Serial No. 08/572,202. This is a *provisional* double patenting rejection since the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. § 103 which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
>
> Subject matter developed by another person, which qualifies as prior art only under subsection (f) or (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

9. Claims 1-11, and 13-29 are rejected under 35 U.S.C. § 103 as being unpatentable over Hollowell, II et al. in view of Watts, Jr. et al.

As per claims 1, 2, and 3, Hollowell discloses the claimed invention including a provision for user input (Fig. 1); a provision for output (Fig. 1); a CPU coupled to the input and output (Fig. 1; col. 4, lines 6-7); the input is a keyboard (Fig. 1; col. 4, lines 42-44); the output is a display device (Fig. 1; col. 4, lines 21-22); a temperature level detector (Fig. 1; col. 4, lines 47-48); and a thermal management system that stops the clock signal to the CPU when the temperature detected exceeds a reference temperature (Abstract; Fig. 2).

However, Hollowell does not teach a CPU sleep manager. Watts teaches that it is known to include a CPU sleep manager (col. 15, lines 16-17). It would have been obvious to one having ordinary skill in the art at the time the invention was made to include the CPU sleep manager as taught by Watts, to monitor the temperature levels in the computer, to prevent excessive temperature which may damage vital components or circuitry.

As per claim 4, Hollowell discloses the claimed invention as above in claims 1, 2, and 3. Watts discloses the CPU sleep manager as above in claims 1, 2, and 3. However Hollowell does not teach a CPU activity detector. Watts teaches that it is known to include a CPU activity detector (Abstract). It would have been obvious to one having ordinary skill in the art at the time the invention was made to include the CPU activity detector as taught by Watts, to monitor the activity by the computer, in which the activity causes energy to be expended resulting in further heat.

As per claim 5, Hollowell discloses the claimed invention as above in claims 1-4. Watts discloses the CPU sleep manager and a CPU activity detector as above in claims 1-4. However Hollowell does not teach a CPU sleep manager stopping the clock signals to the CPU only when the CPU is processing non-critical I/O. Watts teaches that it is known to include stop the clock to the CPU when it is processing non-critical I/O (Fig 2d; col. 10,

lines 7-14). It would have been obvious to one having ordinary skill in the art at the time the invention was made to stop the clock only when the CPU is processing non-critical I/O as taught by Watts, to prevent losing any vital information or processing that may occur during an I/O operation.

As per claim 6, Hollowell discloses the claimed invention as above in claims 1-3. Watts discloses the CPU sleep manager as above in claims 1-3. However Hollowell does not teach a CPU receiving a one of a first clock signal at a first speed or a second clock signal at a second speed and the CPU receives the first clock signal when the temperature is below the reference temperature and the receives the second clock signal when the temperature is greater than or equal to the reference temperature. Watts teaches that it is known to provide first and second clock signals with first and second speeds to the CPU (Fig. 3; col. 15, lines 3-20). It would have been obvious to one having ordinary skill in the art at the time the invention was made to include the above as taught by Watts, to provide different clock speeds based upon the required load of the CPU.

As per claim 7, Hollowell and Watts discloses the claimed invention as above in claims 1, 2, 3 and 6. However Hollowell does not teach a CPU activity detector. Watts teaches that it is known to include a CPU activity detector (Abstract). It would have been obvious to one having ordinary skill in the art at the

time the invention was made to include the CPU activity detector as taught by Watts, to monitor the activity by the computer and it's peripherals, in which the activity causes energy to be expended resulting in further heat.

As per claim 8, Hollowell and Watts discloses the claimed invention as above in claims 1, 2, 3, 6, and 7. However Hollowell does not teach a CPU sleep manager stopping the clock signals to the CPU only when the CPU is processing non-critical I/O. Watts teaches that it is known to include stop the clock to the CPU when it is processing non-critical I/O (Fig 2d; col. 10, lines 7-14). It would have been obvious to one having ordinary skill in the art at the time the invention was made to stop the clock only when the CPU is processing non-critical I/O as taught by Watts, to prevent losing any vital information or processing that may occur during an I/O operation.

As per claim 9, Hollowell and Watts teach the invention as above in claims 1, 2, and 3. However, Hollowell does not teach reducing the clock speed when the detected temperature level is greater than or equal to the reference temperature. Watts teaches that it is known to slow down (reduce) the clock speed (col. 3, lines 48-49). It would have been obvious to one having ordinary skill in the art at the time the invention was made to reduce the clock speed as taught by Watts, to allow for CPUs that cannot have their clocks stopped.

As per claim 10, Hollowell and Watts discloses the claimed invention as above in claims 1, 2, 3, and 9. However Hollowell does not teach a CPU activity detector. Watts teaches that it is known to include a CPU activity detector (Abstract). It would have been obvious to one having ordinary skill in the art at the time the invention was made to include the CPU activity detector as taught by Watts, to monitor the activity by the computer and it's peripherals, in which the activity causes energy to be expended resulting in further heat.

As per claim 11, Hollowell and Watts discloses the claimed invention as above in claims 1, 2, 3, 9, and 10. However Hollowell does not teach a CPU sleep manager stopping the clock signals to the CPU only when the CPU is processing non-critical I/O. Watts teaches that it is known to include stop the clock to the CPU when it is processing non-critical I/O (Fig 2d; col. 10, lines 7-14). It would have been obvious to one having ordinary skill in the art at the time the invention was made to stop the clock only when the CPU is processing non-critical I/O as taught by Watts, to prevent losing any vital information or processing that may occur during an I/O operation.

As per claim 13 and 16, Hollowell discloses the claimed invention, including the temperature level detector, the CPU, and the CPU is part of a computer (Fig. 1; col. 4, lines 3-7) except for activating a hardware selector based upon determining if the

CPU may rest. Watts teaches that it is known to activate a hardware selector based upon determining if the CPU may rest (Abstract). It would have been obvious to one having ordinary skill in the art at the time the invention was made to include the above as taught by Watts, since logic is needed to provide the appropriate clock speeds to the CPU based upon each condition.

As per claim 14, Hollowell and Watts discloses the claimed invention as in claim 13 above. However, Hollowell does not teach the hardware selector applies oscillations to the clock input of the CPU based upon if the CPU is to sleep/rest or if the CPU is active. Watts teaches that it is known to have the hardware selector apply oscillations to the clock input of the CPU based upon the CPU state (Abstract; Fig. 3). It would have been obvious to one having ordinary skill in the art at the time the invention was made to include the above as taught by Watts, since the CPU requires different clock speeds based upon the state of the CPU. A first clock speed is slow if the CPU is in a rest or sleep mode and a second clock speed is fast if the CPU requires activity.

As per claim 15, Hollowell and Watts discloses the claimed invention as in claim 13 above. However, Hollowell does not teach the hardware selector preventing the oscillations for the clock input to the CPU if the CPU is to rest or supplies

oscillations to the CPU at full speed if the CPU is to be active. Watts teaches that it is known to provide full speed to the CPU when it is active and not when it is in sleep/rest mode (Abstract; Fig. 3). Figure 3 shows a circuit in which the D flip-flop in conjunction with the oscillators provide the clock to the CPU. Either a sleep clock speed or a high speed clock can be fed to the CPU, not both signals. It would have been obvious to one having ordinary skill in the art at the time the invention was made to include the above as taught by Watts, since the CPU requires different clock speeds based upon the state of the CPU. A first clock speed is slow if the CPU is in a rest or sleep mode and a second clock speed is fast if the CPU requires activity.

As per claims 17 and 18, Hollowell discloses the claimed invention including monitoring temperature levels in a computer. However, Hollowell does not teach predicting activity and temperature levels relevant to the operation of a CPU within the computer and using the predictions for automatic temperature control. Watts teaches that it is known to predict activity levels within a computer and using the prediction for automatic control and also, remain transparent to the user (col. 3, lines 10-18). It would have been obvious to one having ordinary skill in the art at the time the invention was made to include the above as taught by Watts, since having the capability to predict temperature rises and automatically control them, prior

to the occurrence could prevent premature failure of the CPU or circuit components.

As per claims 19 and 20, Hollowell and Watts teach the disclosed invention as claims 17 and 18 above. However, Hollowell does not teach user modification of automatic activity and temperature level predictions and using modified predictions for automatic temperature control. Watts teaches that it is known to allow user modification of automatic activity level predictions and using the modified predictions for automatic control (col. 3, lines 18-22). It would have been obvious to one having ordinary skill in the art at the time the invention was made to include the above as taught by Watts, since allowing the user to modify temperature levels would allow for different manufacturer's components that have various temperature specifications.

As per claims 21-23, Hollowell teaches a CPU (Fig. 1; col. 4, lines 6-7) and monitoring temperature levels within the computer system (Abstract). However, Hollowell does not teach sampling temperature levels and automatically adjusting the clock of the CPU to maintain temperature levels below a reference temperature, and the adjustments accomplished within CPU cycles and do not affect the user's perception of performance. Watts teaches that it is known to sample level of CPU activity and reduce the speed of the clock to maintain the temperature below

the reference temperature (col. 3, lines 23-25, lines 40-42) and the adjustments do not affect the user's perception of performance (col. 3, lines 42-45). It would have been obvious to one having ordinary skill in the art at the time the invention was made to include the above as taught by Watts, since the temperature levels should remain below manufacturer's specifications for proper operation of the circuit and the speed should be reduced to the CPU when it has minimal load. This speed should be reduced so that a user would not see any adverse effects from the slow down.

As per claim 24, Hollowell teaches a CPU coupled to a clock (Fig. 1) and a monitoring temperature levels within the computer system (Abstract). However, Hollowell does not teach a means responsive to the temperature level for controlling period of time the clock is in an OFF state and the lengths of periods of the time of the clock being appropriate to maintain the temperature below the reference temperature. Watts teaches that it is known to control the periods of the time the clock is in its OFF state, the amount of energy (heat) can be reduced (col. 5, lines 46-47). It would have been obvious to one having ordinary skill in the art at the time the invention was made to include the above as taught by Watts, to allow enough time during the OFF state to allow the cooling of the temperature levels in the computer system to reach acceptable levels.

As per claim 25 and 26, Hollowell and Watts disclose the claimed invention as above in claim 24. However, Hollowell does not teach the energy consumption is at maximum when the length of each period of time the clock is in an OFF state is zero and conversely, the energy consumption decreases as the length of each period of time the clock is in an OFF state increases. Watts teaches that it is known that the energy consumption is at maximum when the length of each period of time the clock is in an OFF state is zero and it's converse (col. 5, lines 48-53). It would have been obvious to one having ordinary skill in the art at the time the invention was made to include the above as taught by Watts, to state as the interval of time goes to zero the clock is always in the ON state and thus at maximum energy and as the interval of time increases the clock is always in the OFF state thus reducing the energy consumption.

As per claim 27, Hollowell and Watts disclose the claimed invention as above in claim 24. However, Hollowell does not teach the periods of time the clock is in an OFF state are constantly being adjusted to maintain the operating temperature of the CPU below the reference temperature. Watts teaches that it is known to constantly adjust the period of the clock while it is in an OFF state (col. 6, lines 2-5). It would have been obvious to one having ordinary skill in the art at the time the invention was made to include the above as taught by Watts, to

regulate the varying temperatures that occur in the computer system to acceptable levels.

As per claim 28 and 29, Hollowell and Watts disclose the claimed invention as above in claim 24. However, Hollowell does not teach the OFF state represents the minimum clock rate at which the CPU can operate and the minimum clock rate may be zero for CPU that can have their clocks stopped. Watts teaches that it is known that the OFF state represents the minimum clock rate at which the CPU can operate and the minimum clock rate may be zero for CPU that can have their clocks stopped (col. 5, lines 14-17). It would have been obvious to one having ordinary skill in the art at the time the invention was made to include the above as taught by Watts, to have a reference to monitor the time period the CPU is in the OFF state and what speed it is running.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.
The following prior art teach a thermal management system which controls the temperature of the computer system by sampling/sensing temperature levels, reducing clock speeds, monitor activity levels, and selecting high clock speeds versus slow clock speeds.

~~Rawson, III et al. (5,535,401)~~ RDD

Chen et al. (5,422,806)

Kenny et al. (5,287,292)

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Rupal Dharia whose telephone number is (703) 305-4003. The examiner can normally be reached on Monday-Thursday from 6:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Harvey, can be reached on (703) 305-9705. The fax phone number for this Group is (703) 308-5358.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-9600.

JACK B. HARVEY
SUPERVISORY PATENT EXAMINER
GROUP 2300

RDD
Rupal D. Dharia
February 7, 1997